AMPLIFIER CIRCUIT WITH OUTPUT DELAY SELECTIVELY CHANGED ACCORDING TO COMMON MODE VOLTAGE LEVEL, ASSOCIATED REPLICA DELAY CIRCUIT AND INTERNAL CLOCK GENERATOR
Application No. NEW - Docket No. SEC.1158
Inventor: Won-ki PARK

FIG. 1 (PRIOR ART)

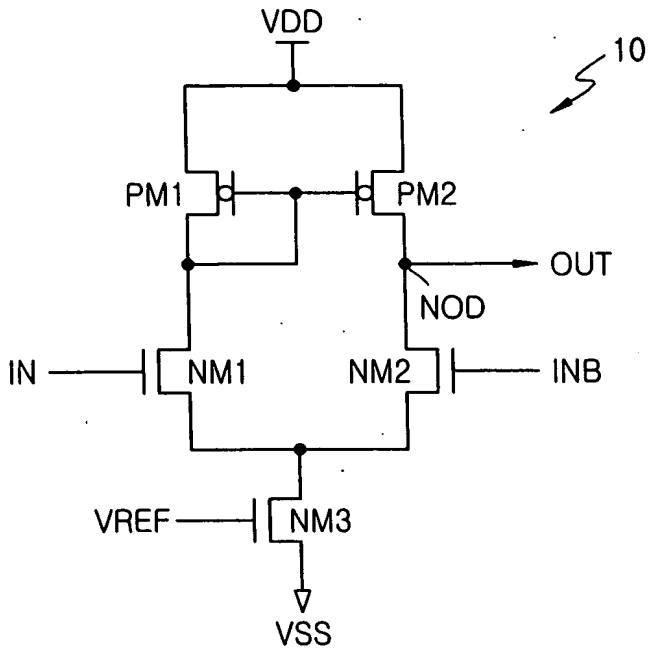

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FIG. 2 (PRIOR ART)

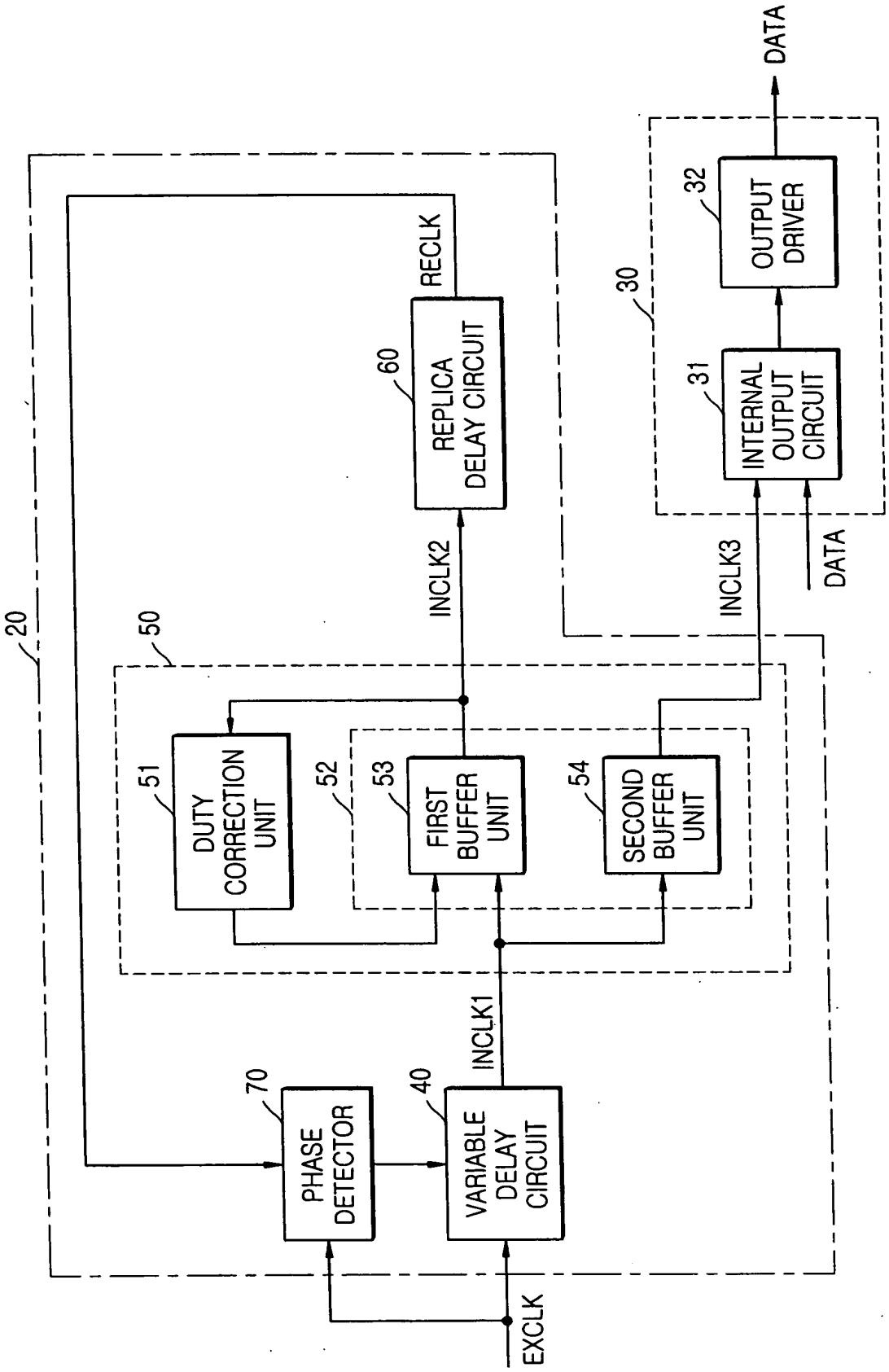

FIG. 3A (PRIOR ART)

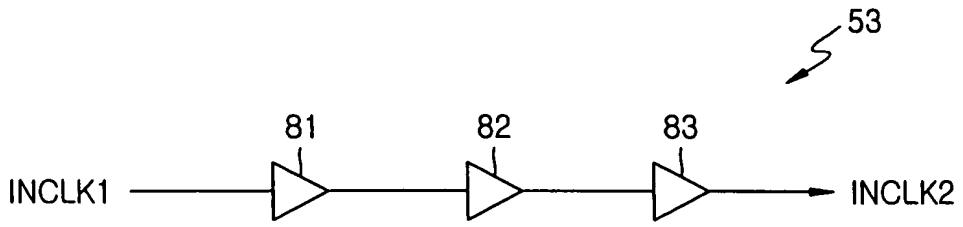

FIG. 3B (PRIOR ART)

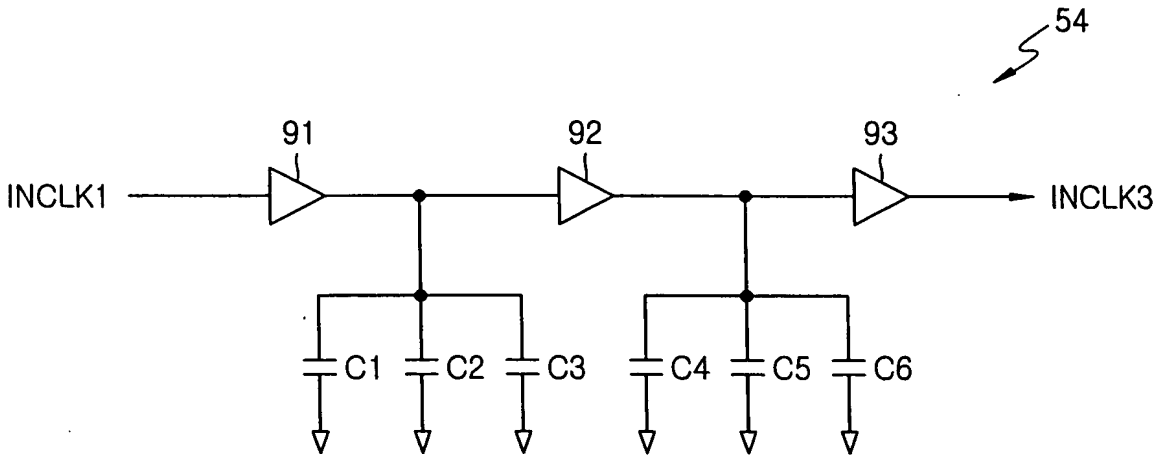

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FIG. 4

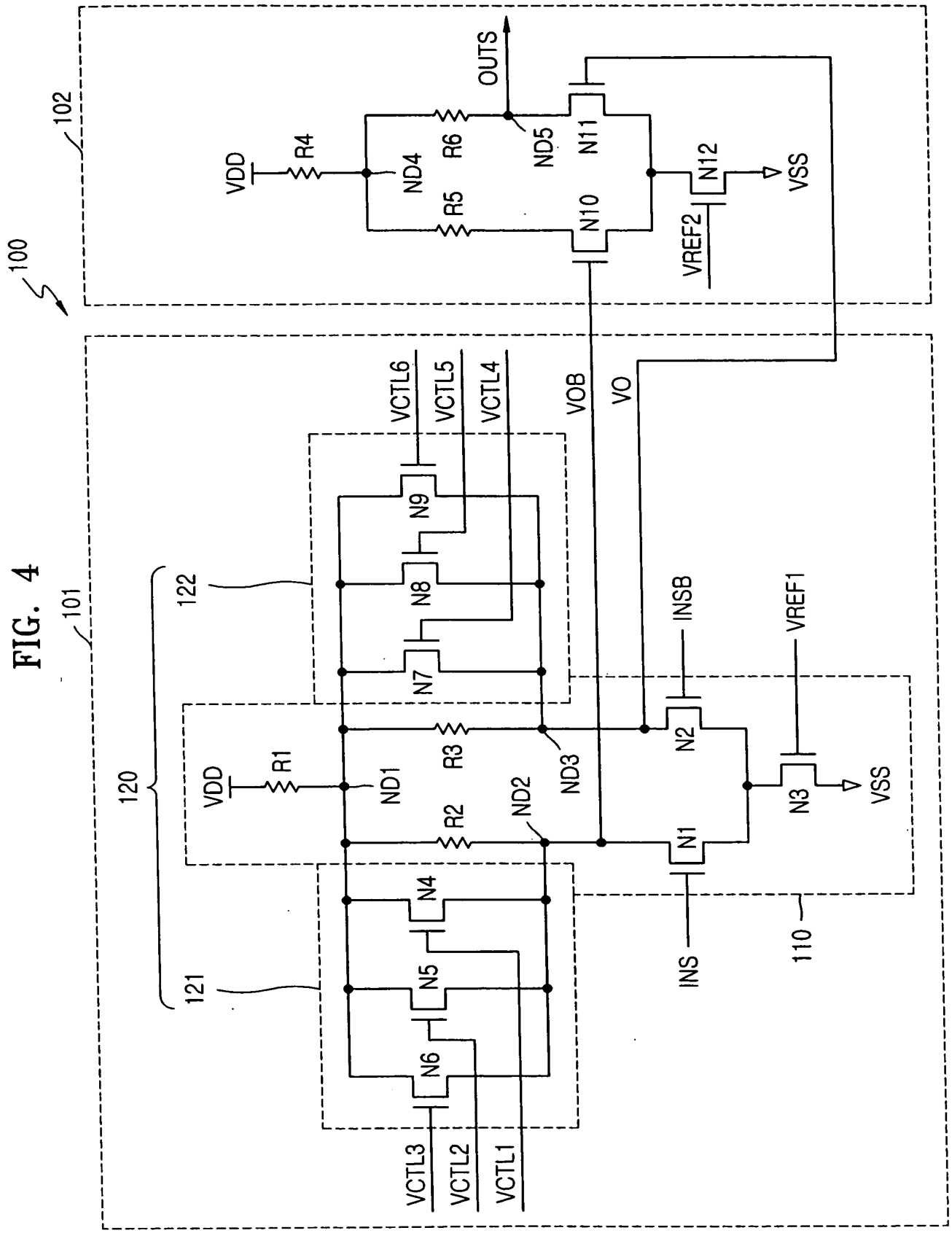

FIG. 5

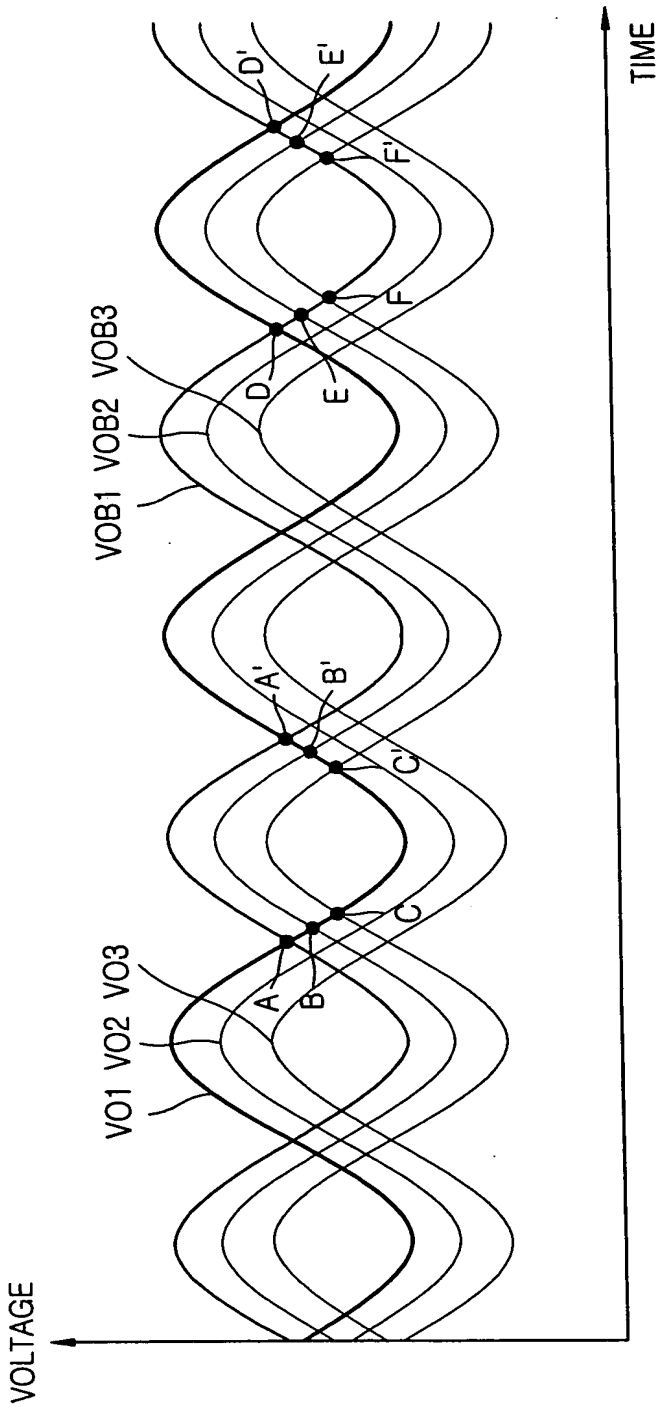

FIG. 6A

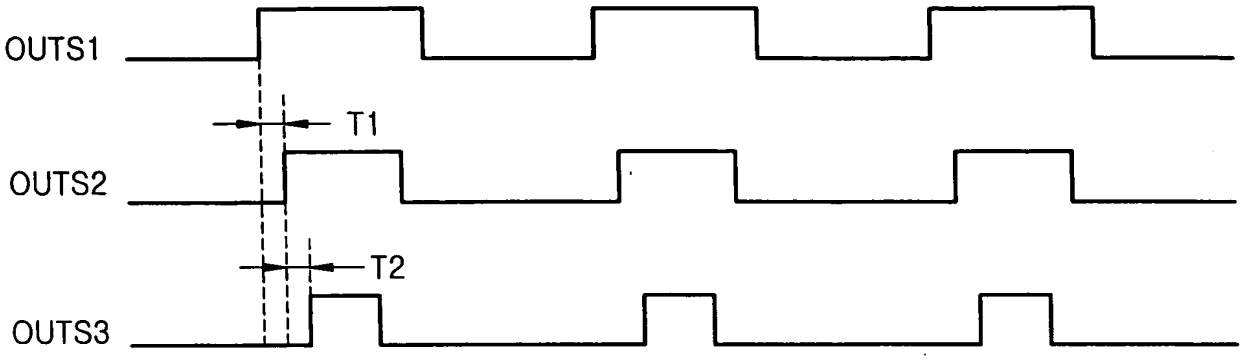

FIG. 6B

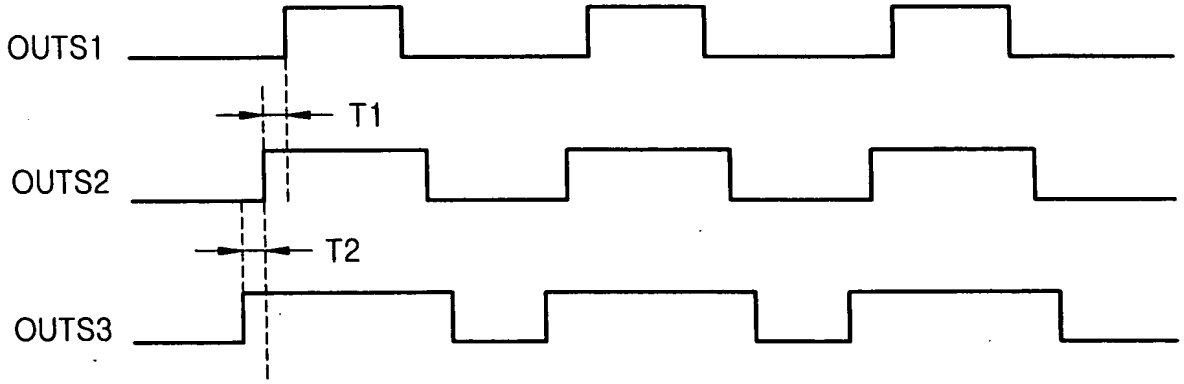

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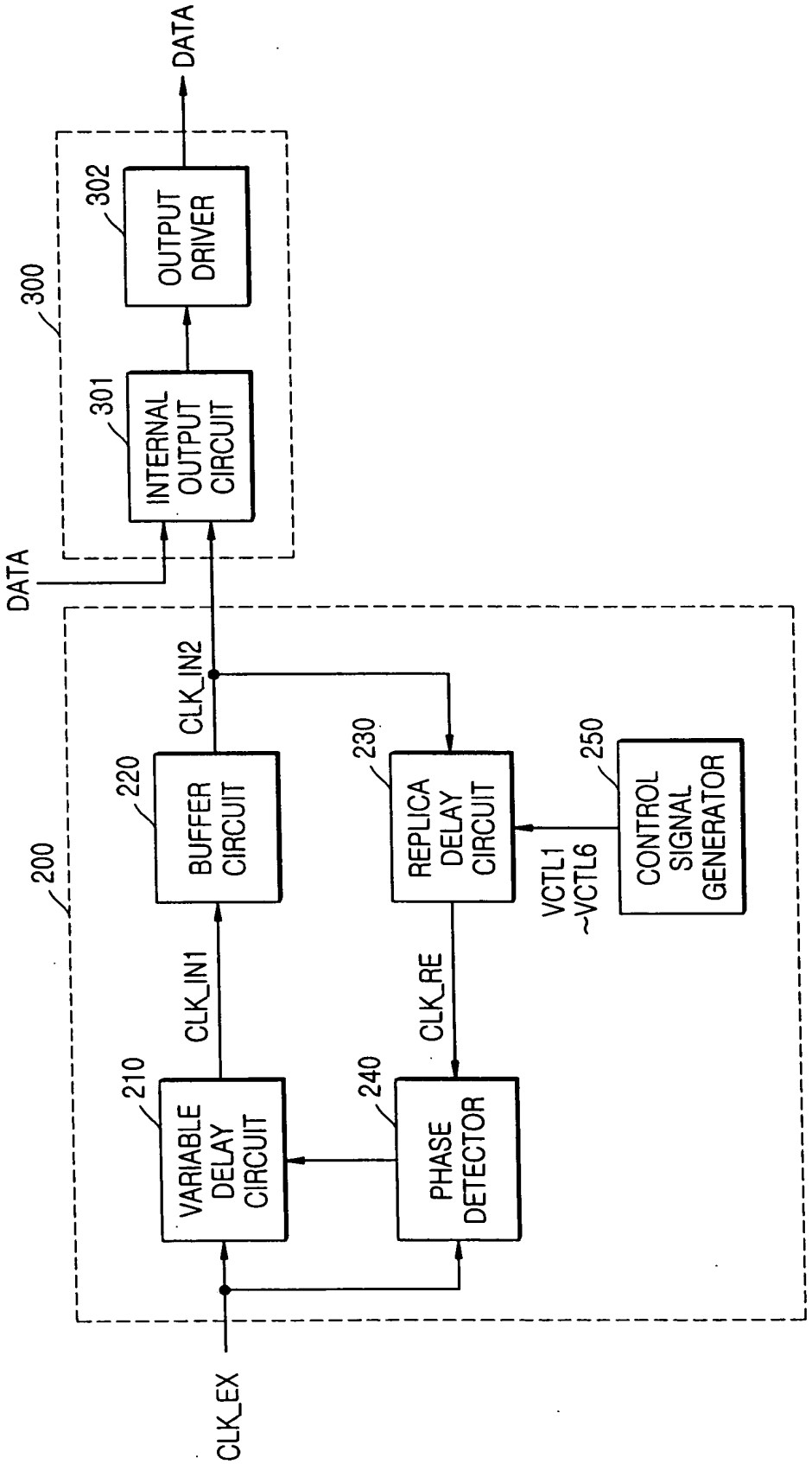
FIG. 7



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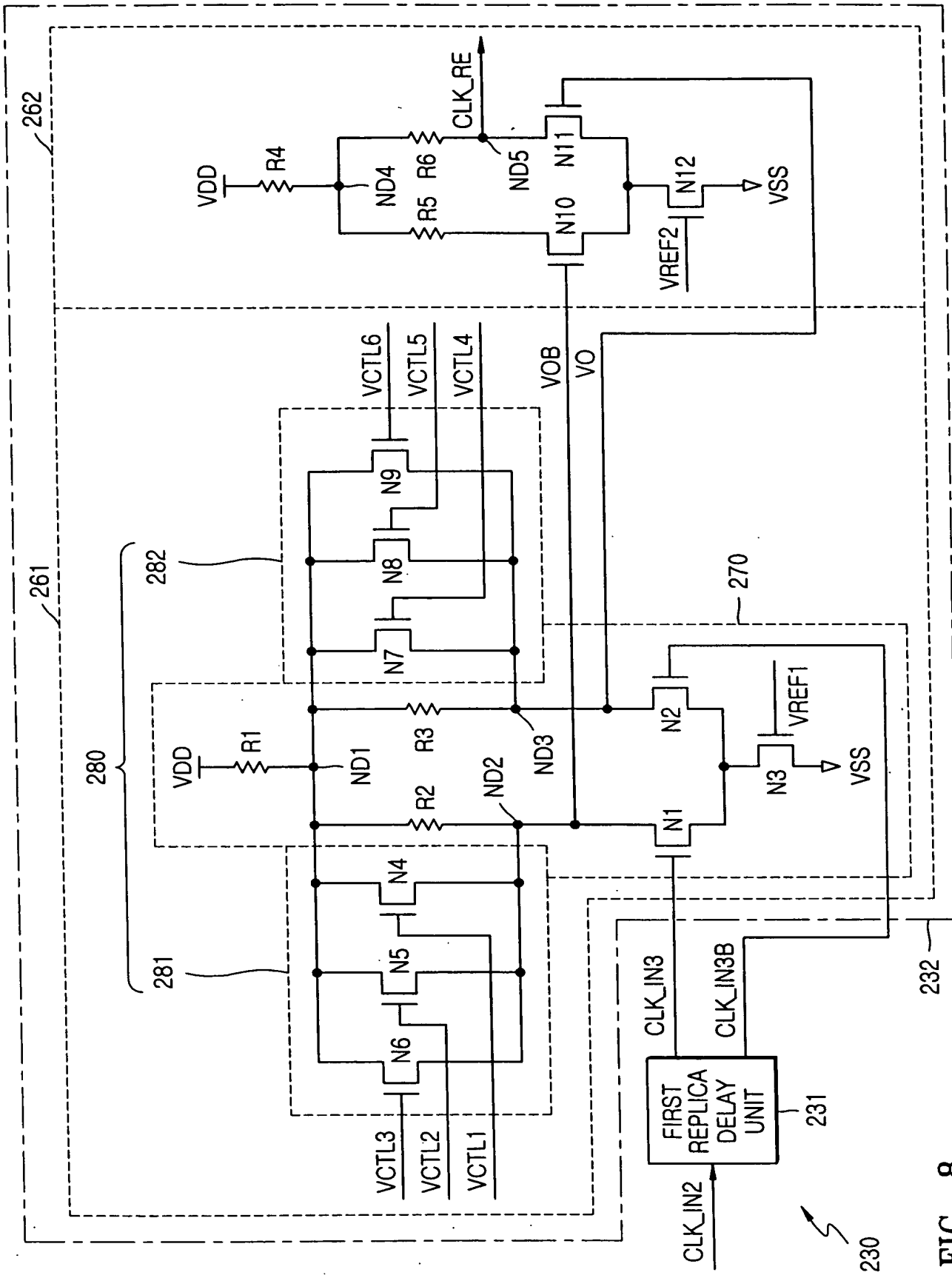

FIG. 8